Stephan Held

Academic career

2008	Dr. rer. nat., University of Bonn
2009 - 2010	Postdoc, Georgia Institute of Technology, Atlanta, GA, USA
2010 - 2013	Junior Professor (W1), University of Bonn
2013 - 2016	Professor (W2), tenure track, University of Bonn
Since 2016	Professor (W2), University of Bonn

Invited Lectures

2006	NATO summer school on combinatorial optimization, Montreal, QC, Canada
2009	Spring School on Mathematics of Chip Design, Hangzhou, China

Research Projects and Activities

“Combinatorial Optimization and Chip Design”,
long-term cooperation funded by IBM Corporation, since 2010

Research profile

My current research focus is on combinatorial optimization and its application in chip design. Here, one of the major problems is the Steiner tree problem, which occurs in various variants. The major problem is to find Steiner trees for fast but economic signal distribution [18, 14, 11], potentially with obstacles [**?**], and subsequent repeater insertion [16]. Steiner trees on a chip cannot be designed independently but are mutually dependent in their space consumption and signal speeds. Here we showed how to to incorporate all constraints into a common resource sharing model and solve its continuous relaxation efficiently [**?**].
Steiner trees occur also in the realization of parity functions and similar commutative functions. Here there are also side terminals besides the major terminals and the problems becomes a two-level Steiner tree problem [2]. However, most logic functions are more complex than parity calculations. One of the most important ones is binary addition, for which we improved the running time for optimizing the depth of carry-bit calculation from cubic to near-linear [5]. Other important aspects of signal speed optimization are the gate placement and sizing [**?**, **?**, **?**, **?**].
A major challenge in chip design is the huge number of design variables and constraints. While some specific subproblems, such as placement, buffering, gate sizing, and routing can be solved more or less well in practice, approaches tackling several of these steps are mostly build on heuristics. We plan to continue the approach for timing-constrained global routing in [**?**] to integrate most design variables into a single global mathematical problem formulation, aiming provably good computer chips.
We will continue to find better structures for logic functions. The carry-bit circuits computed by the algorithm from [5] are fastest possible when restricting to so called prefix gates, which are pre-dominantly used in industry. When abandoning this paradigm, faster adders are possible, but were hardly investigated in the last 40 years. We want to characterize the general best tradeoffs between depth, size, and interconnect complexity for adders and other functions on modern computer chips. A new focus is related to the traveling salesman problem (TSP). The major application of the TSP in practice is the vehicle routing problem, where cities have to be partitioned to multiple salesmen, which visit their bounded number of cities in a tour. The total length of all tours is to be minimized. For this problem it is not even clear whether the separation of the so called subtour inequalities is NP-hard or solvable in polynomial time. A polynomial time algorithm would have immediate positive consequences to many practical applications in logistics. Another interesting question in this respect is the best topology of such a tour network. We want to study the benefit of further sub-partitions.

Editorships

• IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (since 2016)
Member in technical program committees of conferences with published proceedings:
• International Symposium on Physical Design (2014 - 2016)
• International Conference on Computer-Aided Design (2016)

Research Area KL Besides general improvements for optimizing signal delays in chip design [9, 7], we made substantial improvements towards a comprehensive global optimization, consolidating steiner tree packing an signal delay constraints into a common, practically solvable model, [8, 4], and providing new Steiner tree functions for better signal delays and routing [12, 10, 3]. Furthermore, we developed new adder circuits [6, 1], achieving for the first time: an asymptotically minimum depth, linear size and a maximum fanout 2. This is the first major improvement in adder design in more than 30 years!

Supervised theses

Master theses: 13, currently 3
Diplom theses: 2
PhD theses: 3, currently 2

Selected publications

[1] S. Held and S. T. Spirkl. Binary adder circuits of asymptotically minimumdepth, linear size, and fan-out two. *ACM Transactions on Algorithms, to appear*, 2017. arxiv: 1503.08659v2.
[2] Stephan Held and Nicolas Kämmerling. Two-level rectilinear steiner trees. *Comput. Geom.*, 61:48–59, 2017.
[3] Stephan Held and Nicolas Kämmerling. Two-level rectilinear steiner trees. *Computational Geometry*, 61:48–59, 2017.
[4] Stephan Held, Dirk Muller, Rudolf Rotter, Daniel andScheifele, Vera Traub, and Jens Vygen. Global routing with timing constraints. *IEEE Transactions on Computer-Aided Design ofIntegrated Circuits and Systems*, 2017.
[5] Stephan Held and Sophie Spirkl. Fast prefix adders for non-uniform input arrival times. *Algorithmica*, 77(1):287–308, 2017.
[6] Stephan Held and Sophie Spirkl. Fast prefix adders for non-uniform input arrival times. *Algorithmica*, 77(1):287–308, 2017.
[7] Adrian Bock, Stephan Held, Nicolas Kämmerling, and Ulrike Schorr. Local search algorithms for timing-driven placementunder arbitrary delay models. In *Proceedings of the 52nd Annual Design AutomationConference*, page 29. ACM, 2015.
[8] Stephan Held, Dirk Müller, Vera Rotter, Danieland Traub, and Jens Vygen. Global routing with inherent static timing constraints. In *Proceedings of the IEEE/ACM International Conferenceon Computer-Aided Design*, pages 102–109. IEEE Press, 2015.
[9] Stephan Held and Ulrike Schorr. Post-routing latch optimization for timing closure. In *Design Automation Conference (DAC), 2014 51stACM/EDAC/IEEE*, pages 1–6. IEEE, 2014.
[10] Stephan Held and Sophie Theresa Spirkl. A fast algorithm for rectilinear steiner trees withlength restrictions on obstacles. In *Proceedings of the 2014 on International symposium onphysical design*, pages 37–44. ACM, 2014.
[11] Stephan Held and Daniel Rotter. Shallow-light steiner arborescences with vertex delays. In *Integer programming and combinatorial optimization*, volume 7801 of *Lecture Notes in Comput. Sci.*, pages 229–241. Springer, Heidelberg, 2013.
[12] Stephan Held and Daniel Rotter. Shallow-light steiner arborescences with vertexdelays. In *IPCO*, pages 229–241, 2013.
[13] William Cook, Stephan Held, and Edward C Sewell. Maximum-weight stable sets and safe lower bounds forgraph coloring. *Mathematical Programming Computation*, pages 1–19, 2012.
[14] C. Bartoschek, S. Held, J. Maß berg, D. Rautenbach, and J. Vygen. The repeater tree construction problem. *Inform. Process. Lett.*, 110(24):1079–1083, 2010.
[15] Christoph Bartoschek, Jens Held, Stephan andMaßberg, Dieter Rautenbach, and Jens Vygen. The repeater tree construction problem. *Information Processing Letters*, 110(24):1079–1083, 2010.
[16] C. Bartoschek, S. Held, D. Rautenbach, and J. Vygen. Fast buffering for optimizing worst slack and resource consumption in repeater rrees. In *Proceedings International Symposium on Physical Design*, pages 43–50, 2009.
[17] Stephan Held. Gate sizing for large cell-based designs. In *Proceedings of the Conference on Design, Automationand Test in Europe*, pages 827–832. European Design and Automation Association, 2009. Best paper award at DATE'09.

[18] C. Bartoschek, S. Held, D. Rautenbach, and J. Vygen. Efficient generation of short and fast repeater tree topologies. In *Proceedings of the International Symposium on Physical Design*, pages 120–127, 2006.

[19] Stephan Held, Bernhard Korte, Jens Mabetaberg, Matthias Ringe, and Jens Vygen. Clock scheduling and clocktree construction for highperformance asics. In *Proceedings of the 2003 IEEE/ACM internationalconference on Computer-aided design*, page 232. IEEE Computer Society, 2003.